ABSTRACT

A novel device and process is described for an ESD protection device for ESD voltages appearing on IC power voltage bus lines. The invention consists of an ESD protection discharging NMOS with source connected to a first voltage bus line, or Vcc, and having the drain connected to a second voltage bus line, or ground. The NMOS device gate is connected to ground through a diffused resistor assuring the device remains in an off state during normal operation. An unique aspect of the invention is a special diffusion under and around the device drain which lowers the drain to substrate breakdown voltage enabling the ESD protection current discharge to start at a lower voltage than otherwise. This feature reduces voltage stress on the gates of active devices being protected, and enables higher ESD current discharges at the same power level as for devices without the special drain diffusion.